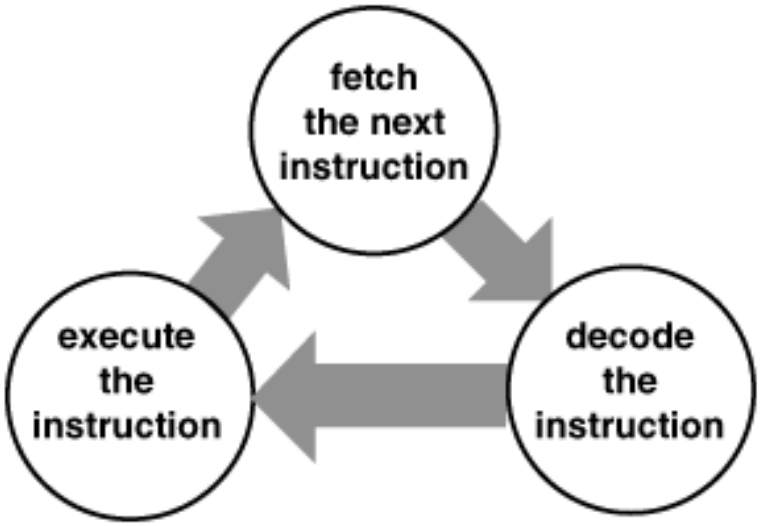
Chapter 5: Computing Components

Stored Program Concept – Ch. 5.2

- von Neumann architecture
  - memory holds both data and instructions (interchangeable)
  - Central Processing Unit (CPU)
    - Arithmetic/logic unit (ALU)
    - Control Unit
  - input, output units

- Fetch-(Decode)-Execute Cycle
  - fetch next instruction (PC determines from where)
  - decode instruction (extract op code, operand address)
  - get data, if needed (operand address determines from where)
  - execute instruction
  - advance PC (program counter)

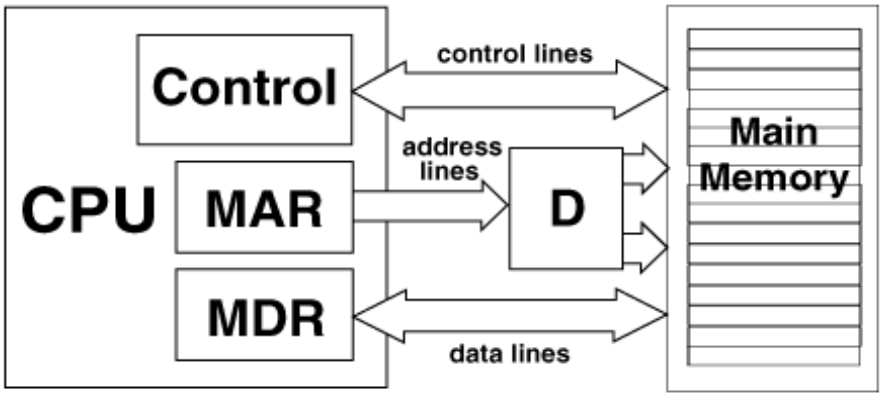


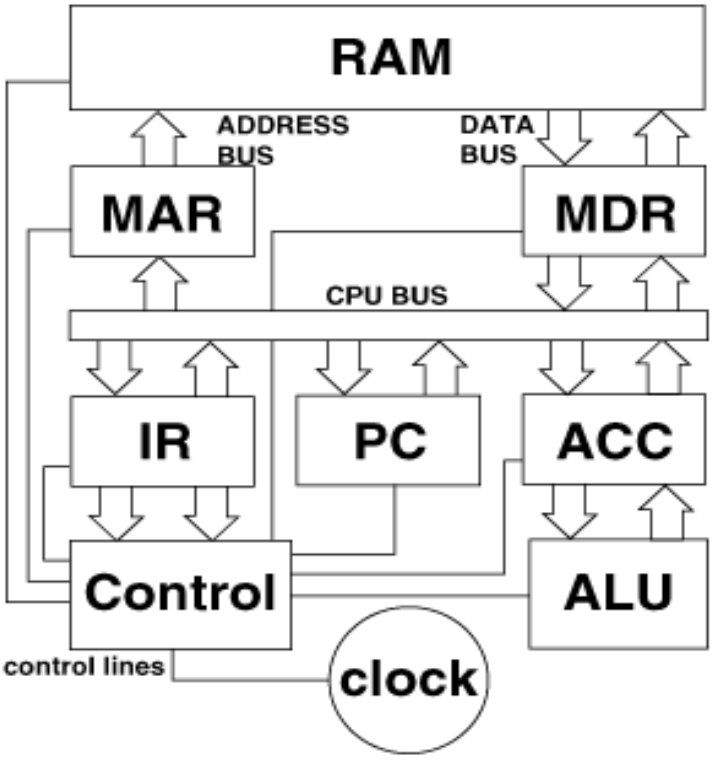
- Generally the faster your computer can get through a fetch-decode-execute cycle, the faster it will perform
- Cycle times are measured in "gigahertz' these days: a billion cycles per second
- PCs these days reach 3.5 gigahertz (3.5 billion cycles/sec.)

Let's design a computer

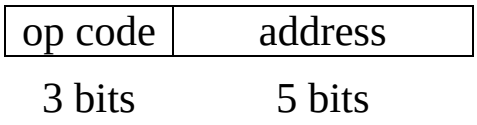
Generic CPU with Registers

Program Counter (PC) [5 bits]
Instruction Register (IR) [8 bits]
Memory Address Register (MAR) [5 bits] ↔ Memory
Memory Data Register (MDR) [8 bits]
Accumulator (A or Acc)





Instruction format: 3-bit op code, 5-bit address



Instructions and their op codes:

000	HALT (HLT)
001	LOAD (LDA)
010	STORE (STA)
011	ADD (ADD)
100	SUBTRACT (SUB)
101	BRANCH (BR)
110	BRANCH ON ZERO (BRZ)
111	BRANCH ON POSITIVE (BRP)

LOAD Instruction (LDA)
- PC → MAR
- MDR → IR
- IR [address] → MAR
- MDR → A
- PC + 1 → PC

STORE Instruction (STA)
- PC → MAR
- MDR → IR
- A → MDR
- IR [address] → MAR
- PC + 1 → PC

ADD Instruction (ADD)
- PC → MAR
- MDR → IR
- IR [address] → MAR
- A + MDR → A
- PC + 1 → PC

HALT Instruction (HLT)
- PC → MAR
- MDR → IR
- stop