Dept. of Computer Science and Engineering
CSE4210 – Architecture and Hardware for DSP
Lab 1
Fast adders

In this lab you will design, synthesize, and simulate a carry ripple adder, and a ~~conditional sum adder~~. Carry select adder. Then use simulation to determine the time it takes to complete the addition using these two adders.

Introduction

Carry ripple adders wee introduced in CSE3201 and you should be very familiar with it.

For ~~conditional sum adder~~ carry select adder, look at the notes to see how it is constructed, as promised, I am including here an example using 7-bit addition

Note that in the first group (S(0),C(0)) we calculate the sum and carry for individual bits.

Then in the second group (S(1),C(1)) we combine together each 2 bits of the first group.

Then we combine two groups in the first to produce third group (S(2),C(2)), then two groups to produce the last one S(3),C(3)

	A	1	1	0	1	1	0	1
	B	0	1	1	0	1	1	0
C=0	$S_i(0)$	1	0	1	1	0	1	1
	$C_i(0)$	0	1	0	0	1	0	0
C=1	$S_i(1)$	0	1	0	0	1	0	0
	$C_i(1)$	1	1	1	1	1	1	1
C=0	$S_i(1)$	1	0	1	0	0	1	1
	$C_i(1)$	0	1		1		0	
C=1	$S_i(1)$	0	1	0	0	1	0	0
	$C_i(1)$	1	**1**		1		1	
C=0	$S_i(2)$	0	0	1	0	0	1	1
	$C_i(2)$	1			1			
C=1	$S_i(2)$	0	1	0	0	1	0	0
	$C_i(2)$	1			0			
C=0	$S_i(3)$	0	1	0	0	0	1	1
	$C_i(3)$	1						
C=1	$S_i(3)$	0	0	1	0	1	0	0
	$C_i(3)$	1						

Specifications

- Design your adder for 12 bits
- Perform timing simulation on your design, considering the wors cast, what is the delay for both adders?

Report

In your report, draw the schematic diagram of the circuit and include simulation results.