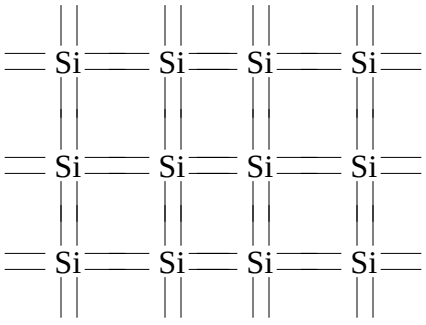
Digital Logic Design

CMOS

MOS



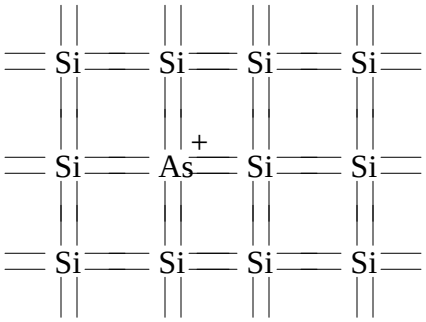
Silicon Si (group IV) forms a covalent bonds with for adjacent atoms (3-D crystals).

All of its valence electrons (4) are involved in chemical bonds -- poor conductor

Conductivity can be raised by introducing a small amount of impurities (dopants)

MOS

n-type

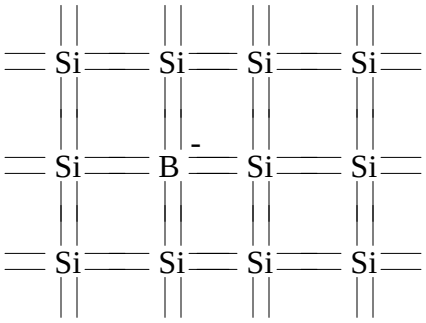


A group V dopant such as Arsenic has 5 valence elctrons, it replaces an Si atom in the lattice and bonds to 4 neighbors.

The 5th valence electron is loosely bound to the arsenic atom.Thermal vibration at room temperature is sufficient to set the electron free to move leaving a positively charged As^+

MOS

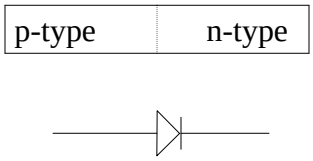
p-type



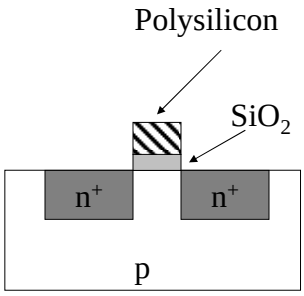
A group III dopant such as Boron has 3 valence electrons, it replaces an Si atom in the lattice and bonds to 4 neighbors.

Baron can borrow an electron from a neighboring Si atom, which can borrows an electron from a neighboring atom and so on, the hole (+) can move round.

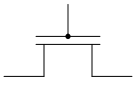
p-n junction



MOSFET Transistors



n-MOS

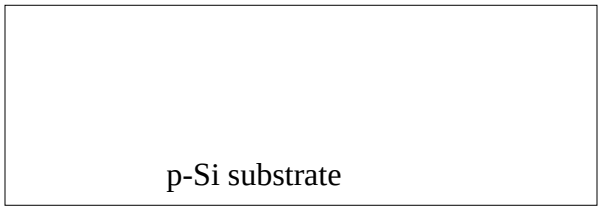


The body is generally grounded

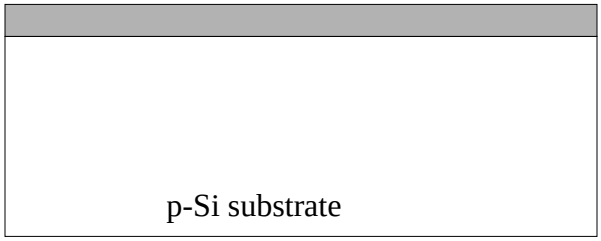
The p-n junction in the source and drain are reverse-biased, if the gate is grounded, no current flows

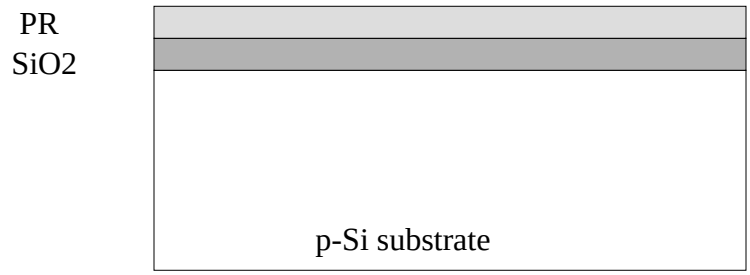
If the gate is +ve enough, an electric field is created that attract electrons to the surface.

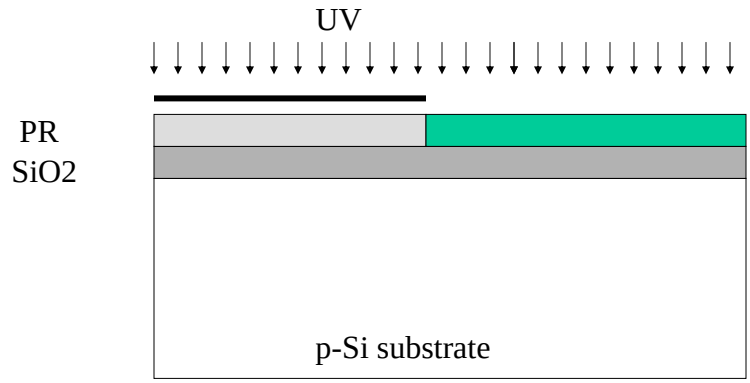
Electrons outnumbers the holes, and a thin region under the gate ***channel*** is inverted to be n-type and current can flow

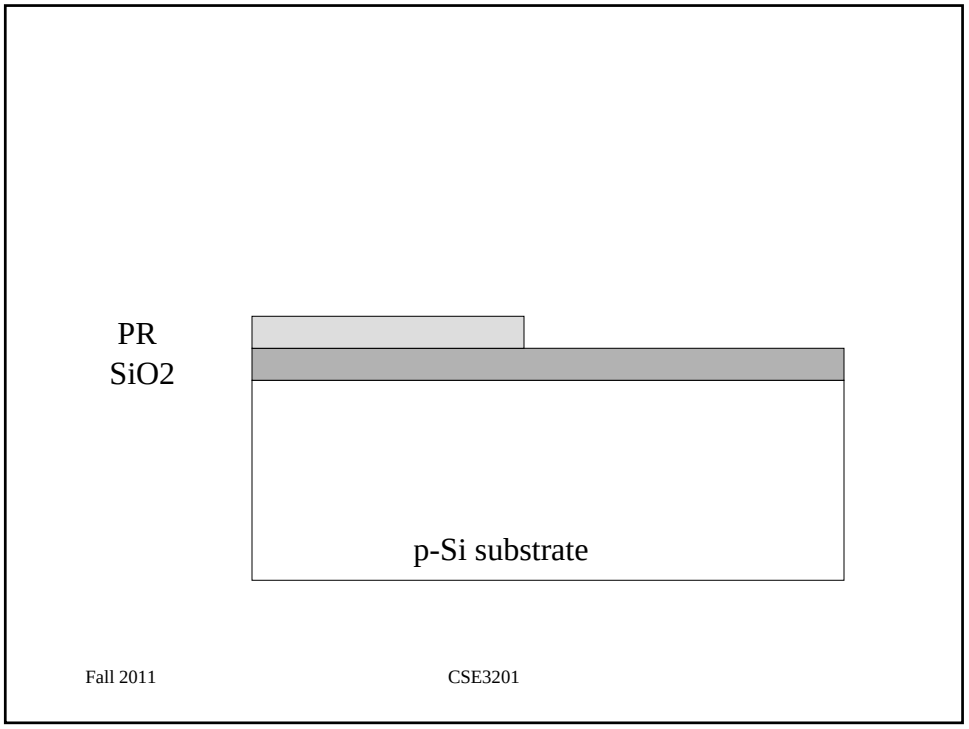


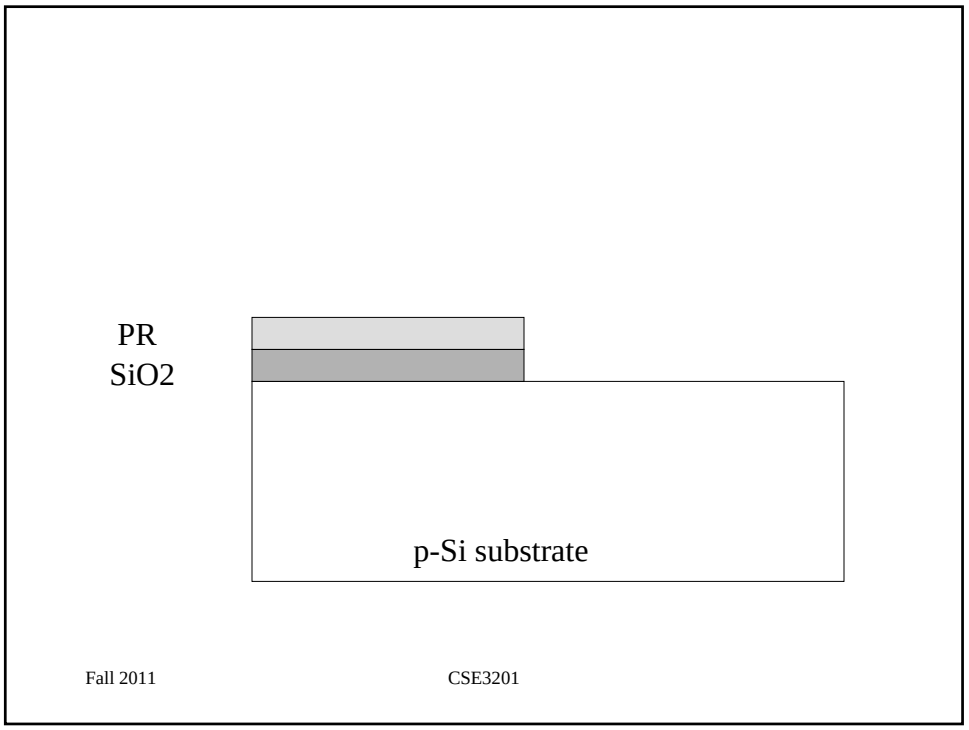
SiO2

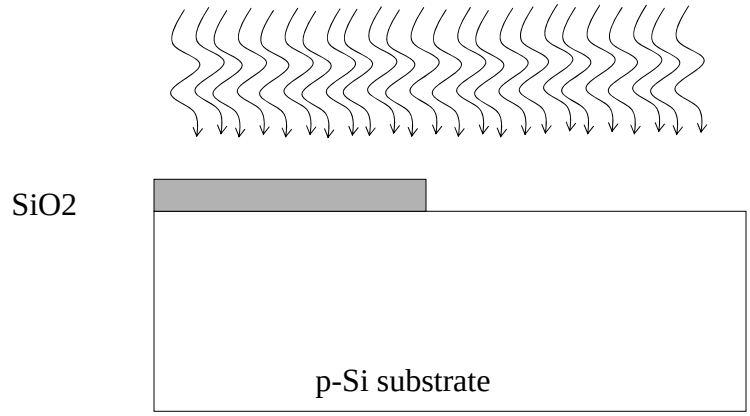


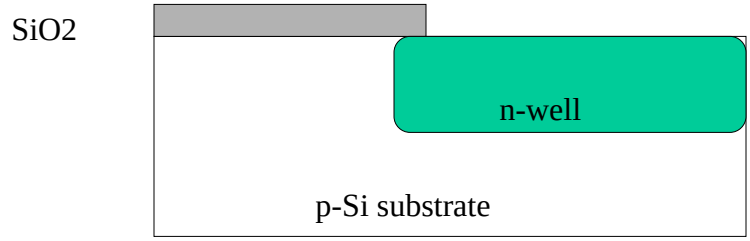

PR
SiO2
p-Si substrate

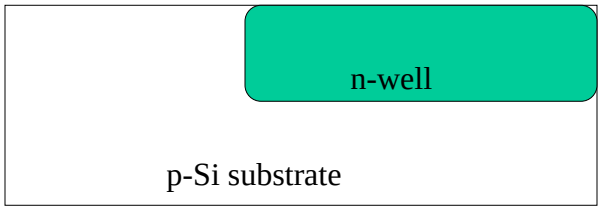

UV
PR
SiO2
p-Si substrate


PR
SiO2
p-Si substrate


PR
SiO2
p-Si substrate


SiO2
p-Si substrate


SiO2
n-well
p-Si substrate

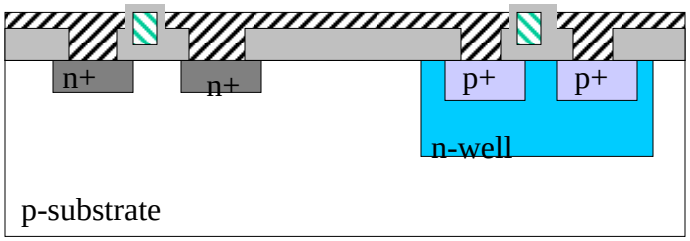


Inverter

p+ n+ diffusion SiO_2

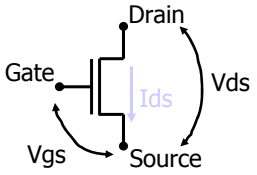
Poly

Metal

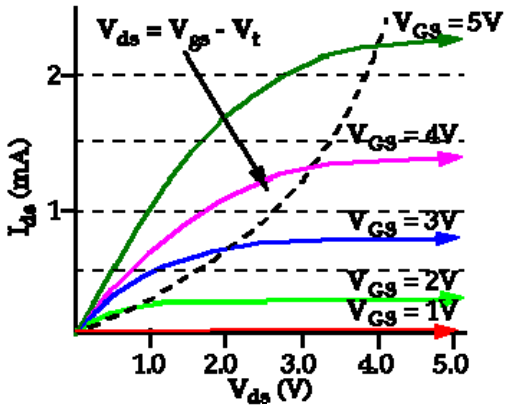


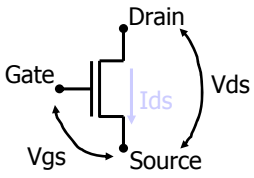
N-Type MOS Transistor

- Cut-off Region
  - Vgs – Vt $\leq$ 0
  - No current (Ids) between drain and source
- Linear (or Ohmic) Region
  - 0 < Vds < Vgs – Vt
  - Ids is a function of Vgs and Vds
  - Ids = β*[(Vgs-Vt)*Vds – Vds*Vds/2]
- Saturation Region
  - 0 < Vgs – Vt < Vds
  - Ids is independent of Vds
  - Ids = (β/2)*(Vgs-Vt)^2
  - β = process factor * (W/L)
- Vt : Threshold voltage, a function of materials, doping, insulator thickness, etc.



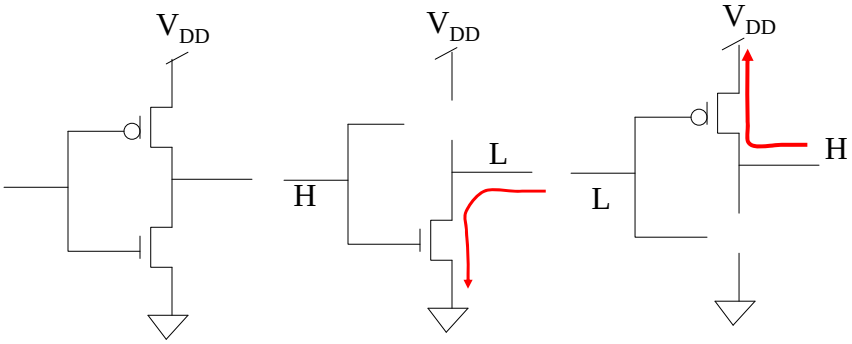
N-type MOS Transistor





N-type MOS Transistor

Inverter



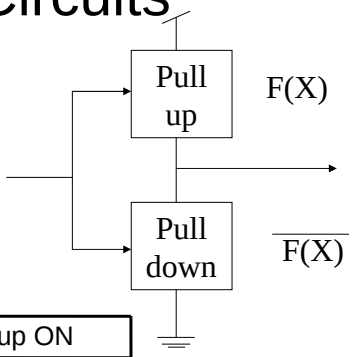
CMOS Circuits

- In general, CMOS circuits consists of 2 components, pull up network, and a pull down network.
- The pull up and pull down networks are duals, (sufficient but not necessary condition) to construct one from the other:
  - Exchange NFETS for PFETS and vice versa
  - Exchange series connections with parallel connections and vice versa
- The pull up (pull down) network represents the computations of the function's 1(0)-valued outputs.

CMOS Circuits

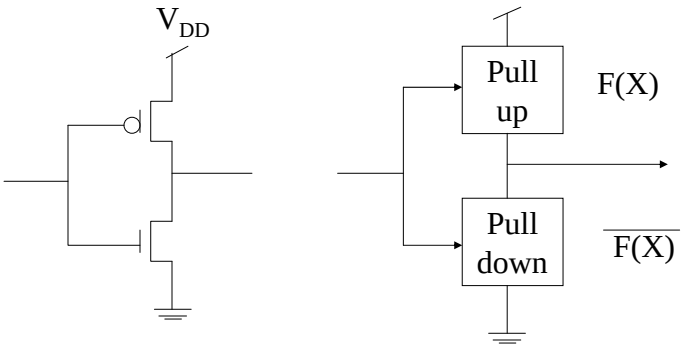
- nMOS transistors pass a strong 0
  - But degraded or weak 1
- pMOS transistors pass a strong 1
  - But degraded or weak 0
- Therefore, nMOS transistors are best for the "pull-down" network

CMOS Circuits

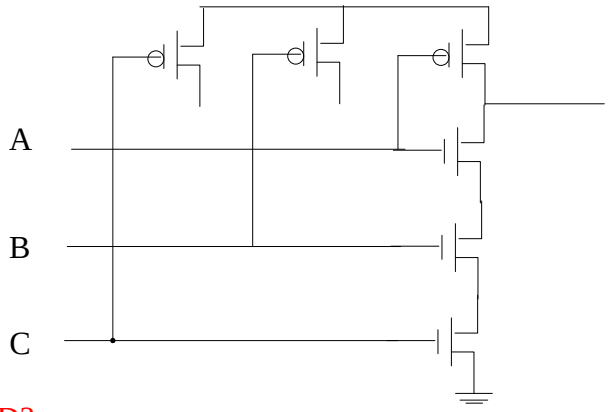


	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)

Inverter

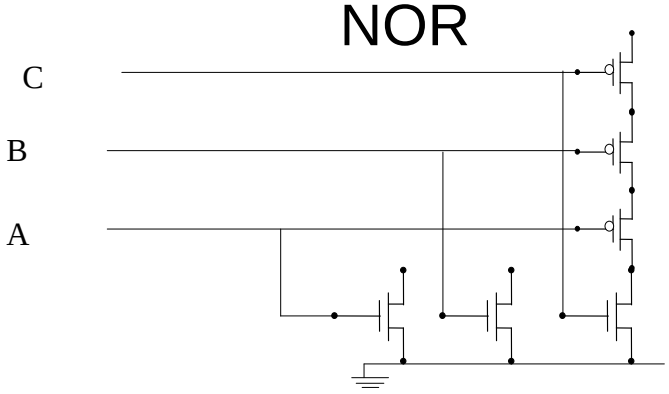


NAND



What about AND?

NOR

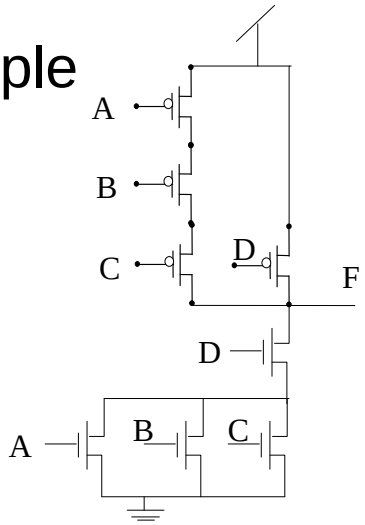


Example

$$F = \overline{(A + B + C) \bullet D}$$

$$F = \overline{(A + B + C)} + \overline{D}$$

$$\overline{F} = (A + B + C) \bullet D$$

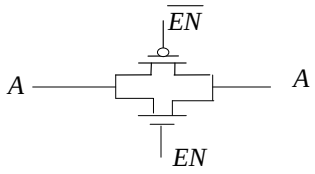


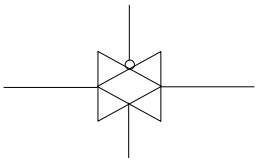
Example

$$F + AB + C + \overline{D}E$$

Transmission Gates

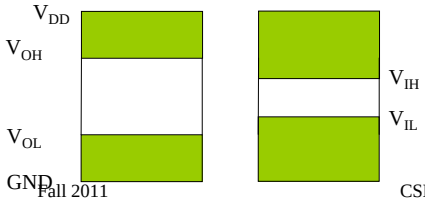
- nMOS transistors pass '0' well, but '1' poorly ($V_{DD} - V_{TN}$)
- pMOS is the opposite low voltage is not '0' but $|V_{TP}|$





Noise Margin

- V_{IH} = minimum HIGH input voltage
- V_{IL} = maximum LOW input voltage
- V_{OH} = minimum HIGH output voltage
- V_{OL} = maximum LOW output voltage



$NM_L = V_{IL} - V_{OL}$

Why do we need margin?

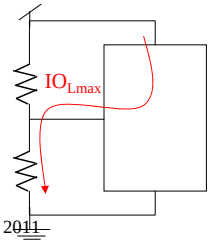
Typical CMOS vs. TTL

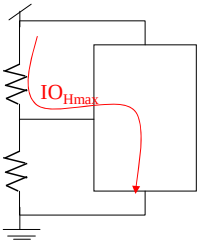
TABLE 8-9 Input/output voltage levels (in volts) with $V_{DD} = V_{CC} = +5$ V.

	CMOS							TTL		
Parameter	**4000B**	**74HC**	**74HCT**	**74AC**	**74ACT**	**74AHC**	**74AHCT**	**74**	**74LS**	**74AS**
V_{IH}(min)	3.5	3.5	2.0	3.5	2.0	3.85	2.0	2.0	2.0	2.0
V_{IL}(max)	1.5	1.0	0.8	1.5	0.8	1.65	0.8	0.8	0.8	0.8
V_{OH}(min)	4.95	4.9	4.9	4.9	4.9	4.4	3.15	2.4	2.7	2.7
V_{OL}(max)	0.05	0.1	0.1	0.1	0.1	0.44	0.1	0.4	0.5	0.5
V_{NH}	1.45	1.4	2.9	1.4	2.9	0.55	1.15	0.4	0.7	0.7
V_{NL}	1.45	0.9	0.7	1.4	0.7	1.21	0.7	0.4	0.3	0.3

Fan out

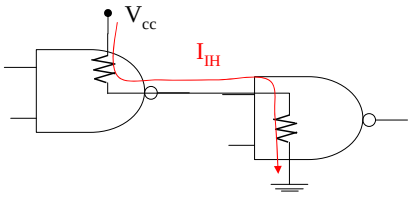
- I_{OLmax} = the max. current that the output can sink in the LOW state and still maintain an output voltage no greater than V_{OLmax}.
- I_{OHmax} the maximum current that the output can source in the HIGH state and still maintain an output voltage no less than V_{OHmin}

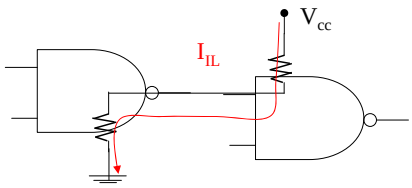




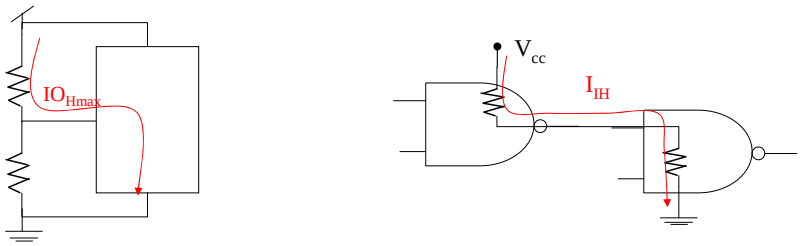
Fan Out

- I_{IH} is the current that the device sinks with a logic "1" at the input (20 mA).
- I_{IL} is the current that the device can sink with a logic "0" at the input. (-0.1 mA)





Fan Out

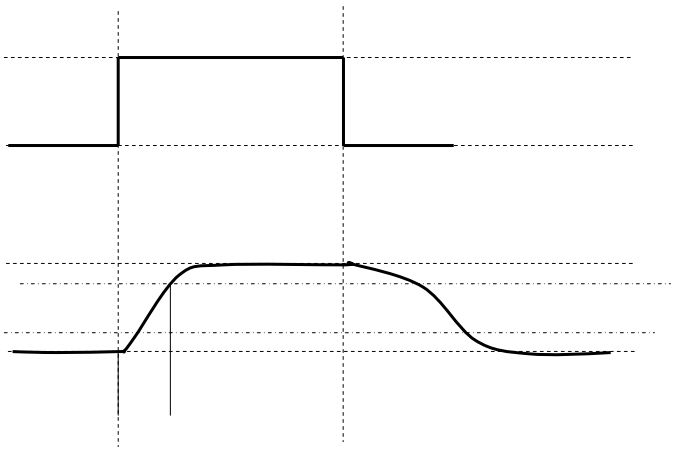


$$\text{Fan out} = \max\left(\frac{I_{OH\,\max}}{I_{IH}}, \frac{I_{OLmac}}{I_{IL}}\right)$$

Practical Consideration

- What happens when you overload a CMOS
  - V_{OL} may increase beyond V_{OLmax} What is wrong with that?
  - V_{OH} may drop beyond V_{OHmin} What is wrong with that?
  - Output rise and fall times may increase (slower operation)
- What to do with *unused inputs*?
  - Never leave unconnected
  - Either tie them together, tie them HIGH or LOW

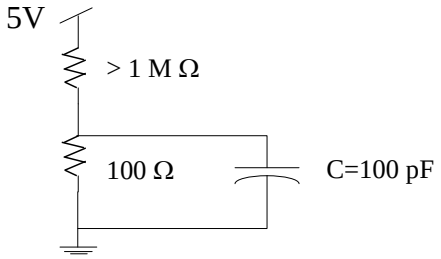
Transition Time



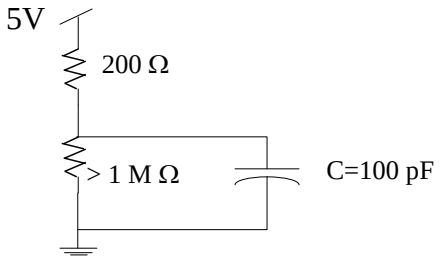
CMOS Dynamic Behavior

- When a MOS transistor switches from HIGH to LOW or vice versa, it discharges or charges a capacitor
- That depends on the time constant of the (dis)charging circuits
- Time constant τ=RC

HIGH to LOW



LOW to HIGH



What is R and C

- Manufacturers do not specify the transistor "ON" resistance.
- Could be estimated as follows (keep in mind it is voltage controlled resistance which is controlled by V_{gs})

$$R_{p(on)} = \frac{V_{DD} - V_{OH\min T}}{|I_{OH\max T}|} \qquad R_{n(on)} = \frac{V_{OL\max T}}{I_{OL\max T}}$$

Current Spikes

- WHEN CMOS transistors switches between LOW and HIGH, current flows between VDD and ground through the partially ON p and n transistors, that is known as current spikes.
- Systems that use CMOS circuits require *decoupling capacitors* between VDD and ground at least one within an inch or so from each chip.

The Design Process