Dept. of Computer Science and Engineering
CSE3201 – Digital Logic Design
Lab 7
Stopwatch

In this lab you will design, implement, and test a stop watch.

Specifications

- The stop watch counts seconds and one tenths of a second to a maximum of 99.9 seconds (you need 3 7-segment displays to display the output).
- KEY[0] is a global reset switch, when pushed it sets the time to 00.0, but the clock does not start counting.
- KEY[1] is a "go" switch, when pushed the stop watch either starts counting and displaying, or continue counting or displaying according to the rules for "pause" mentioned next.
- KEY[2] is a pause switch, when pushed the stopwatch pauses counting and displaying, if KEY[1] is pushed after KEY[2], it starts counting and displaying again
- KEY[3] is another pause switch, but in this case the display freezes at the time KEY[3] was pushed, but the clock continue to count in the background. If KEY[1] is pushed, the clock updates the time with the correct time and continues to count and display. For example if you pushed KEY[3] when the display was 10.2, the display freezes at 10.2. If after 2 seconds you pushed KEY[1], then as soon as you push KEY[1] the display shows 12.2 (10.2 + the 2 seconds pause) and continue counting and displaying.

Pre-Lab Work

Complete your design using Verilog, show the program to the TA before starting

Lab report

See the guidelines for the lab report on the Lab section of the course web page. In your report you have to justify the design decisions you made in your design.