Dept. of Computer Science and Engineering
CSE3201 – Digital Logic Design
Lab 4
Adders/Subtractors

In this lab you will design, implement, and test a binary adder/subtractor. The design could be done at the behavioral level or gate level.

Specifications

- The inputs to your circuits are 2 4-bit numbers (A and B) in 2's complement format and another 1-bit input (op bit) to indicate if the operation is an addition (A+B) or subtraction (A-B).
- The output is a 4-bit number in 2's complement format (either A+B, or A-B) depending on the op bit) and a valid bit (V-bit). The V bit is set to 1 if the result is valid, otherwise is set to 0 (if there is an overflow).
- Do not use any predefined circuits, you have to do your design from scratch.

Pre-Lab Work

Complete your design using Verilog, show the program to the TA before starting

Lab report

See the guidelines for the lab report on the Lab section of the course web page. In your report you have to justify the design decisions you made in your design.
State in your report the maximum time your circuit takes to add/subtract any two numbers?
How did you get that maximum time?