Dept. of Computer Science and Engineering
CSE3201 – Digital Logic Design
Lab 3
Reaction Timer

In this lab, you will design a little more complicated system than the previous 2 labs. The design could be done at the behavioral level (there is no need to design any circuits, that will be done later).

Pre-Pre-lab

This step is to help you do the lab. Do not submit it. It is just my attempt to push you to take a hierarchical approach to solve the problem.

Design a counter that displays its value on two of the 7-segment displays. The counter will increment its value by one each time you push KEY [3]. The updated value will be displayed on the 7-segment display as a 2 HEX digits.
One way to implement this problem is to divide it into two modules. A HEX_DISP module that will take a 4 bit binary number as an input, and produces the value of the 7 segments in order to represent this number as a HEX number (similar to what you did in Lab 2). The top level module will instantiate this module and a 16-bit *reg* variable will be incremented with the negedge of KEY [3].

Problem definition:

For the reaction timer lab, you measure the time between pushing two different keys. First you push KEY[2] followed by KEY[1]. Measure the time period between these 2 pushes and display the result on the 7-segment display set (more than one display) in milliseconds in HEX.

You have to be sure that KEY[2] is pushed before KEY[1]. If KEY[1] is pushed first, display some error message (could be sitting the displayed value to 0, or turning on a LED as an indication of error).

The idea is to start a counter running with a specific rate (the board has a CLOCK_50 which a 50 MHz clock that you can use for that, there is also a 27MHz clock). Then you capture the value of the counter when KEY[2] is pushed, and when KEY[1] is pushed. Be sure that KEY[2] is pushed first, subtract these two values, convert it to milliseconds and display it.

There are some design decisions that you have to make here

- What rate the counter should run at (you have to capture very quick reaction time).
- How to be sure that KEY[2] is pushed first? keep in mind that eventually the counter will reach its maximum value and then becomes all zeroes again.
- What is the maximum reaction time that your system can measure?

Bonus:

As a 10% bonus, you can display the number in decimal rather than hex.

Pre-Lab Work

Complete your design using Verilog, show the program to the TA before starting

Lab report

See the guidelines for the lab report on the Lab section of the course web page. In your report you have to justify the design decisions you made in your design.