Dept. of Computer Science and Engineering CSE3201 – Digital Logic Design Lab 1

In this lab, you will get familiar with the DE2 board from Altera. This is your first lab, so there is no pre-lab.

Follow the instructions in the Verilog entry tutorial to do the following and the schematic entry tutorial (you have to do this twice, once using Verilog entry method and one using schematic entry method).

Implement the function $F = x + \overline{y} z + \overline{z} \overline{x}$

Compile the function to be sure it is error free

Use the simulator to simulate the function

Download the circuit to the board in both modes (JTAG and Active Serial Mode), test it

Deliverables

You have to show to the TA the simulation of your circuit, and the circuit working on the board.