Dept. of Computer Science and Engineering
CSE3201 – Digital Logic Design
Lab 9

A combinational lock.

In this lab, you will design a combinational lock. The lock needs a specific password in order to open. There are two modes of operation, in the first you set the password, in the second you enter the password, if correct the lock opens.

Problem Statement.

Setting the password.

The password is entered on switches SW_3.. SW_0 (4 bits password). By making SW_4 goes high the password is locked.

Open the lock

To open the lock, enter the passwd on SW_3.. SW_0, while SW_5 is high, pushing SW5 to low (0) will open the safe if the passwd is correct. Opening the lock means one of the 7-segmnet displays will show "1" if the combination is wrong, the 7-segment display shows "0".
You should be able to change the passwd by making SW_4 low, then set the switches, finally make SW_4 high to lock in the passwd.

Pre-Lab Work

Complete your design including a schematic diagram for the circuits and Verilog code; show the program and the circuit to the TA before starting

Lab report

See the guidelines for the lab report on the Lab section of the course web page.

Extra Credit:

Make your lock *locks* after three wrong attempts. If that happen, the lock can not open again by changing the passwd. Of course you have to have a global reset switch in order to take you out of this situation. Also when you start the circuit, be sure you will not be in this *locked* state (a global reset switch can do that).