Dept. of Computer Science and Engineering
CSE3201 – Digital Logic Design
Lab 5

Design a circuit to display the binary number represented by the switches
SW_3 SW_2 SW_1 SW_0 on the seven segment display according to SW_5
If SW_5 =1 the number is displayed in octal on 2 displays.
IF SW_5 = 0 the number is displayed as hex number on one display.

When using the 7-segment display to display hex numbers, the B and 8, D and 0 have the same segments ON. You have to think of a way to distinguish between B and 8, D and 0.

You have to use the Q-M method for one of the functions you are minimizing.

Pre-Lab Work

Complete your design using Verilog, show the program to the TA before starting

Lab report
See the guidelines for the lab report on the Lab section of the course web page. For this lab, you have to add the following to your lab report.

- The truth tables for all your functions you used in your design
- The tabular method showing the minimization of the adder circuit.