Dept. of Computer Science and Engineering
CSE3201 – Digital Logic Design
Lab 10

Pulse detection.

In this lab you will design a circuit that displays on the 7 segment display the number of 0-to-1 transitions on a positional switch when the control is high. When the control is low, it keeps the last number displayed and does not change it with the 0-to-1 transitions. A reset switch resets the count to 0 and displays it.

Specifications
The pulses are applied using SW0
KEY0 is used as a reset switch. If pushed the count is reset to 0 and displayed.
SW1 is used as the control switch. If it is LOW the system stops counting the pulses, if HIGH the system counts and displays the pulses on the 7-segment display.
A maximum count of 9 is O.K.

Pre-Lab Work

Complete your design including a schematic diagram for the circuits and Verilog code; show the program and the circuit to the TA before starting. The state machine representing the problem should be ready before you start in the lab.

Lab report

See the guidelines for the lab report on the Lab section of the course web page.