Dept. of Computer Science and Engineering

CSE3201 – Digital Logic Design

Laboratory Report Guidelines

Lab reports are due one week after the lab, at the beginning of the next lab session. The lab reports should be typed, handwritten reports will not be accepted by the TA. Lab reports should contain the following

Cover page: The cover page should include your name, student ID, The name of the course, the date the report submitted, and the lab number and title.

Introduction: Describe in your own words the lab problem.

Design: Describe your own design, schematic diagram (if any), and the Verilog code. If you are using multi modules in your design, give the design of every module and the system block diagram. Also if you used any interface circuitry describe it in details.

Simulation: The testing strategy, the waveforms you used in your simulation and why did you choose these inputs, the expected output and the output of the simulation.

Extra: Any problem that you faced during the design and testing of the lab if any.