Question 1 **(4 points)**
Consider the following MIPS code

```
S1    LOAD      R1, 84(R2)
S2    ADD       R8, R1, #24
S3    SUB       R2, R4, R1
S4    OR        R6, R8, R7
S5    ADD       R8, R2, R8
S6    XOR       R2, R7, R9
S7    STORE     0(R8), R2
```

S1 → S2 True
S2 → S4 T
2 → 5 WAW
2 → 5 T
2 → 7 T

Identify each dependence by type; put your answer in the form Si → Sj (type) meaning Sj depends on Si and the type is (type)

3 → 7 T

<u>Question 2</u> (4 points)

Assume that a program running on a processor A with a clock speed of 1.2 MHz and it takes 64 seconds to complete.

In order to speedup the execution time, a coprocessor for FP operations is used. Assume that it takes 2 cycles to send data to the coprocessor, and two cycles to get back the results. Following is the number of cycles required to do FP operations on the processor and the coprocessor, and the percentage of time (when the FP operations are done on the processor) that the CPU spends in the different FP operations

OP	**Processor**	**Coprocessor**	**% of time**
FP ADD	20	2	10
FP MUL	50	6	20
FP DIV	80	10	25

What is the time to execute the program using a coprocessor?

ADD on Coprocessor $2+2+2=6$ $S_{P1}=\frac{20}{6}$

MUL $6+2+2=10$ $S_{P2}=\frac{50}{10}=5$

DIV ~~80~~ $10+2+2=14$ $S_{P3}=\frac{80}{14}$

$$\text{Total Speedup} = \frac{1}{\frac{0.1}{SP1}+\frac{0.2}{SP2}+\frac{0.25}{SP3}+(0.45)}$$

$$\text{new Time} = \frac{64}{\text{Total speedup}}$$

<u>Question 3</u> (4 points)

Consider a system with 2 level cache,

L1	Hit time = 1 cycle	Hit rate = 95%
L2	Hit time = 4 cycles	Hit rate = 70%
Main memory	Block transfer time = 40 cycles.	

What is the average memory access time considering two alternatives?

a) L1 and L2 are accessed in parallel
b) L1 and L2 are accessed in sequence
c) What are the advantages and disadvantages of the above two cases?

in ⓐ we start accessing L2 with L1, if miss in L1, we saved one cycle

ⓐ Access time = $0.95 + 0.05\,(1 + 0.3 \times \underset{\text{4 for part b}}{3} + 0.7 \times \overset{44}{\cancel{43}})$

4 for part b

ⓐ is faster but more Energy.

<u>Question 4</u> (6 points)

A CPU with a CPI of 2 with a perfect cache, and 1 nsec. cycle time. The specification for the cache and main memory is as follows.

Cache

64KB 2-way set associative write back cache with a hit time of 1 cycle, and a miss rate of 5%. On the average, 30% of the blocks in the cache are dirty. The block size is 32 bytes.

Memory

In order to access the memory, it takes 4 cycles to send the address, then 4 cycles to read/write data. The memory is 2-interleaved with 128-bit bus to the cache.

Assume there are 1.3 memory accesses per instruction; what is the CPI of the machine taking the memory access into consideration.

memory access time for a block (32 bytes)

$4 + (4 + 4) = 12$ cycles.

memory access time $= 1 + 0.05\,(12 + \overset{\text{write back}}{\nearrow}\!\!0.3 \times 12)$

Question 5 (8 points)

```
Loop:     L.D       F0,0(R1)       ;get an array element
          ADD.D     F4,F0,F2       ;Add a constant to the array element
          S.D       F4,0(R1)       Store back the result
          DADDUI    R1,R1,#8       ;increment the index
          BNE       R1,R2,Loop     ;end of array?
```

Consider a 2-issue superscalar using Tomasulo's algorithm without speculation.
Show at what time each instruction is issued, starts execution, finishes execution, uses memory (1 cycle) and writes back the results on the CDB.
For the memory, assume that the load store unit has its own integer ALU for effective address calculation, which takes one cycle, and the memory access takes one cycle. For the rest of the functional units

Integer	1 cycle
FP add	3 cycles
Memory access	1 cycle

Assume there is only one reservation station at each functional unit.

instruction	issue	start	ends	memory	WB
L.D F0,0(R1)	1	2	2	3	4
ADD.D F4,F0,F2	1	5	7	—	8
S.D F4,0(R1)	2	3	3	9	—
DADDUI R1,R1,#8	2	3	3	—	5
BNE R1,R2,Loop	3	6	6		
L.D F0,0(R1)	4	7 ~~6~~	7 ~~6~~	8 ~~7~~	9
ADD.D F4,F0,F2	4	10	12	—	13
S.D F4,0(R1)	5	14	14	15	—
DADDUI R1,R1,#8	5	7 ~~6~~	~~6~~ 7		8 ~~7~~
BNE R1,R2,Loop	6				

<u>Question 6</u> (6 points)

Consider a 1 KB cache, 4-way set associative, with a block size of 16 bytes, and an address space of 20 bytes.
Show the number of bits in the offset, index, and tag parts of the address
Consider the following access pattern
Use **LRU** replacement policy

Similar to HW3

```
ABCDC
ABCD9
910D2
ABD92
91228
956D1
956D6
```

1. How many misses?

2. How many blocks are in the cache after the above access pattern?

You do not need to show the contents of the cache, but it will help you get partial points if you make a simple calculation mistake

Question 7 (4 points)
Consider a distributed memory system with a write invalidate snooping cache protocol. Consider also the following sequence of memory references.

P1 reads block x
P3 reads block y
P1 writes block y
P5 reads block y
P1 reads block x
P4 writes block x

After the end of the sequence.
What is the state of blocks x and y?
Which caches contain block x and/or y?

<u>Question 8</u> (4 Points)

Consider a paged virtual memory with 16KB page size, and a 32-bit address space. How many page faults after the following memory references. Assume that we started with all pages on disk.

```
2 6 A 8 6 A C 4
2 6 A 4 6 2 8 0
2 6 A 4 5 A C 6
3 2 F C 6 A C 8
2 6 A C 6 2 4 0
2 6 A C 2 0 0 0
2 6 B D 2 B D D
2 6 B D 0 2 2 0
```