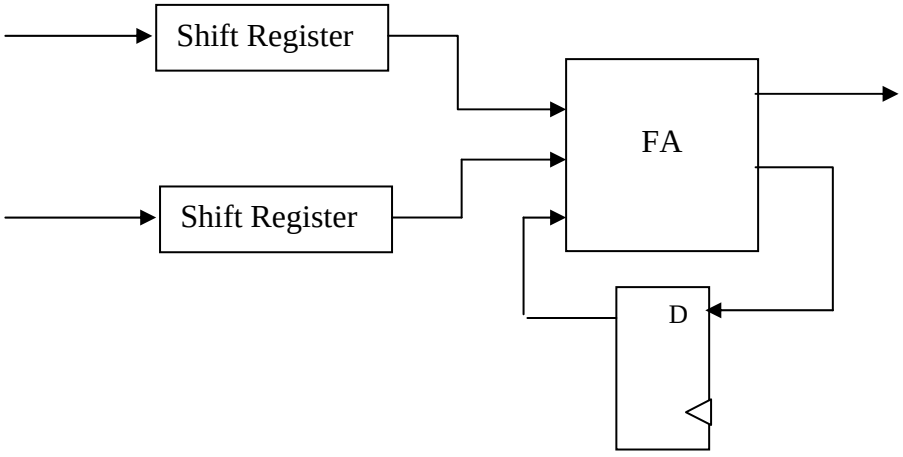
Dept. of Computer Science and Engineering
CSE3201 – Digital Logic Design
Lab 9

## *Part I*

In this lab, you will design a serial adder similar to the one in Fig 6.5 in the book. A block diagram is shown below. The diagram does not show the clock or reset connection.




- The two numbers to be added are 4-bit each.
- The inputs (reset and 2 4-bit numbers are entered from 9 positional switches). The output is shown on 2 7-segment displays.
- A GO signal should be used to add the numbers and display the result.
- After the result is displayed, the result stays there to the next GO (one way of doing that is to design a finite state machine that will be ON for 4 cycles exactly, and then goes to OFF state and stays there up to the next GO).
- You can add one more input to the design if you want.

## *Lab report*

See the guidelines for the lab report on the Lab section of the course web page. For this lab, you have to add the following to your lab report.

- First, your design. How did you approach this problem? Initial block diagram for your solution.
- The truth tables for all your functions you used in your design
- Timing simulation of your circuit, showing the signals on the input and output pins. From the simulation calculate the worst case delay from changing one of your switches until the result is displayed on the 7-segment display