Dept. of Computer Science and Engineering
CSE3201 – Digital Logic Design
Lab 7

Part I

In this lab, you will design a synchronous sequential circuit with 5 inputs, A,B,C,D and RESRT to do the following.
The output of the circuit is a 7 segment-display.
The RESET input displays 0 on the display.
The first button pushed (first input set/reset) of A,B,C, or D display 1,2,3, or 4 on the screen (A displays 1, B displays 2, ...).
The second and consecutive buttons pushed do not change the display (it is basically the first button pushed wins the display, and is displayed until reset is pushed).

Lab report

See the guidelines for the lab report on the Lab section of the course web page. For this lab, you have to add the following to your lab report.

- First, your design. How did you approach this problem? Initial block diagram for your solution.
- The truth tables for all your functions you used in your design
- Timing simulation of your circuit, showing the signals on the input and output pins. From the simulation calculate the worst case delay from changing one of your switches until the result is displayed on the 7-segment display