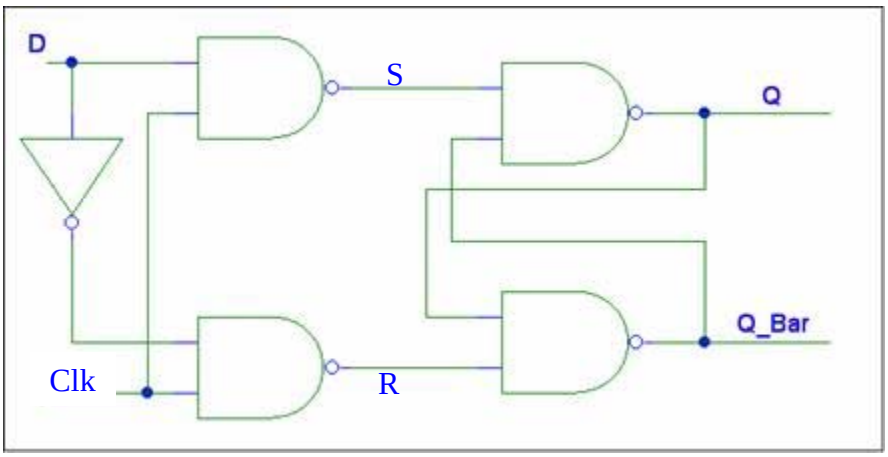
Dept. of Computer Science and Engineering
CSE3201 – Digital Logic Design
Lab 6

Part I

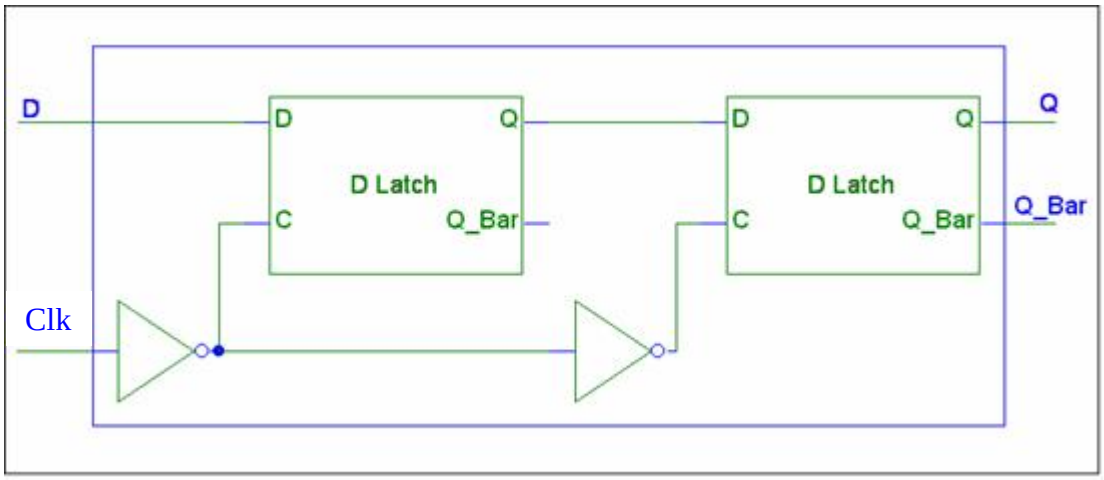
The figure below shows a clocked S-R latch. If the clock is High, D is allowed in to activate the S and R inputs of the latch, if clock is 0, D is blocked and S and R are 1, which does not change the output of the latch.



Write the Verilog code for the above circuit, prepare the appropriate waveforms in order to fully test it.
Implement the circuit on the board and test it.

Part I I

A D Flip-Flop changes its output only at the edges of a cock. The figure below shows a D-FF.



Using the previously designed module, implement the above circuit. Use the appropriate waveforms to test it.
Implement it on the board and test it.

Part III

In the lecture, we showed how to use 2 cross coupled inverters to make a simple latch. We also discussed how to make an oscillator (clock) using this circuit.
Write Verilog code to implement a simple clock using the above circuit. Simulate it.
Does it work ? why or why not?
Can you get it to work using simple modifications to the circuit?
What is the period of this clock?

Lab report

See the guidelines for the lab report on the Lab section of the course web page. For this lab, you have to add the following to your lab report.

- The truth tables for all your functions you used in your design
- The tabular method showing the minimization of the adder circuit.
- Timing simulation of your circuit, showing the signals on the input and output pins. From the simulation calculate the worst case delay from changing one of your switches until the result is displayed on the 7-segment display