Dept. of Computer Science and Engineering
CSE3201 – Digital Logic Design
Lab 5

In this lab, you will compare between two designs for an 8-bit adder.
Design a module for a full adder (3 bits input, and 2 bits output).

- First use the design given in the lecture.
- Do your own design using Quine-McClusky multiple output methods (for s and c).

Compare the hardware cost and the maximum propagation delay of the above 2 circuits.

Then, use the fastest one to design an 8-bit adder. What is the maximum propagation delay and hardware cost of the adder?

Finally, design a carry-lookahead 8-bit adder, what is the hardware cost and maximum propagation delay for the adder.

Use the modules designed in the previous labs in order to test your circuit and show the result on a 7-segment display (limit the testing to only 1 display that is the maximum sum should be less than 10).

Pre-Lab Work

Complete your design using Verilog, show the program to the TA before starting

Lab report

See the guidelines for the lab report on the Lab section of the course web page. For this lab, you have to add the following to your lab report.

- The truth tables for all your functions you used in your design
- The tabular method showing the minimization of the adder circuit.
- Timing simulation of your circuit, showing the signals on the input and output pins. From the simulation calculate the worst case delay from changing one of your switches until the result is displayed on the 7-segment display