Dept. of Computer Science and Engineering
CSE3201 – Digital Logic Design
Lab 4

In this lab, you will use a\the previously designed multiplier, binary to 7-segment display modules in order to design a more complicated function.
Use the previous code you wrote as a module, **do not cut and paste it in your design**.
Design a circuit to perform both addition and multiplication, use the module you wrote in lab 3 for multiplication. Write a module to perform addition, and another circuit to choose what to send to the 7-segment display (either the output of the adder or multiplier). A switch is used for this, if the switch is 0, the 7-segment displays the result of the addition, if it is 1, it should display the result of the multiplication. Use the Quine-McClusky method to minimize the design of the adder (**No need to use multiple output minimization, just do it one function at a time**).

Pre-Lab Work

Complete your design using Verilog, show the program to the TA before starting

Lab report

See the guidelines for the lab report on the Lab section of the course web page. For this lab, you have to add the following to your lab report.

- The truth tables for all your functions you used in your design
- The tabular method showing the minimization of the adder circuit.
- Timing simulation of your circuit, showing the signals on the input and output pins. From the simulation calculate the worst case delay from changing one of your switches until the result is displayed on the 7-segment display