Dept. of Computer Science and Engineering
CSE3201 – Digital Logic Design
Lab 3

Design a multiplier circuit to multiply 2 2-bit binary numbers (0-3) and display the result on the 7-segment display (0-9).
In this lab, you will not use any adders or multipliers, just a combinational circuit that takes 2 2-bit numbers and produce the result on the 7-segment display.

Use K-map in order to minimize your equations. The inputs are from SW0 SW1 for the first number, and SW2 SW3 for the second one. The output is one of the 7-segment displays on the board.

Lab 2 describes how to use the 7-segment display

Pre-Lab Work

Complete your design using Verilog, show the program to the TA before starting

Lab report

See the guidelines for the lab report on the Lab section of the course web page. For this lab, you have to add the following to your lab report.

- The truth tables for all your functions
- K-maps for all the functions and the minimized expression
- Timing simulation of your circuit, showing the signals on the input and output pins. From the simulation calculate the worst case delay from changing one of your switches until the result is displayed on the 7-segment display