York University
Dept. of Computer Science and Engineering
Fall 2006

CSE4210 **Hardware and Architecture for DSP**

Midterm

Monday, Nov. 29th 2006 5:30-7:00pm **(1.5 Hours Only)**

Last Name _____ First name _____

ID _____

Instructions to students:

Answer all questions.
Marks are shown in front of each question number.
Be neat and clean while drawing your logic, block, or state diagrams.

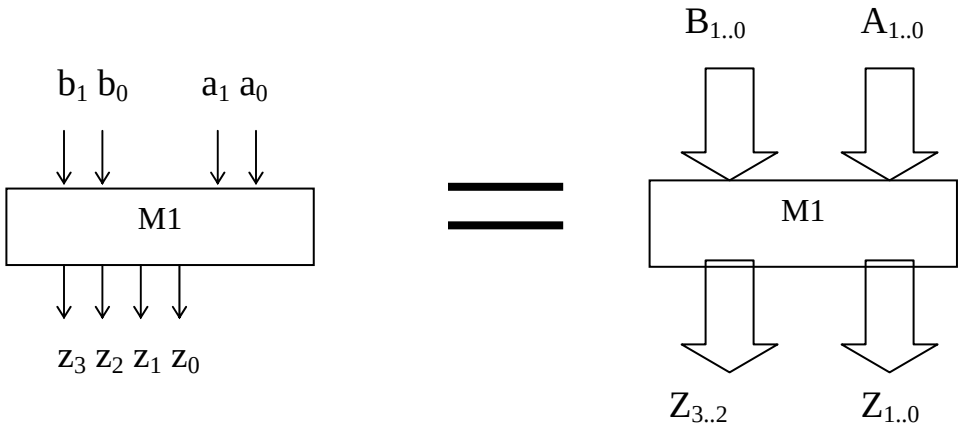
This examination consists of **FIVE** questions

Problem	Points
1	/10
2	/6
3	/6
4	/8
5	/8
Total	/38

Problem 1 (10 points)

Multiply one 4-bit number ($b_3\, b_2\, b_1\, b_0$) by a 3-bit number ($a_2\, a_1\, a_0$) using a 2-bit by 2-bit multiplier. The 2-by-2 bit multiplier is shown below.

1. Show the connection of the input to the multiplier inputs, and the multiplier output to the adder's input. Finally show the result of the multiplication



How many 2-by-2 multipliers do you need? (**1 point**)

How many adders do you need? What is the dimension of each adder? (**3 points**)

Show the circuit. Show the connection between input, multipliers, adders and output (**6 points**)

Problem 2

Implement a 16-bit 2's complement multioperand adder with one level Carry Save Adder (**4 points**)

Estimate the time it will take to add 100 numbers. (**2 points)**

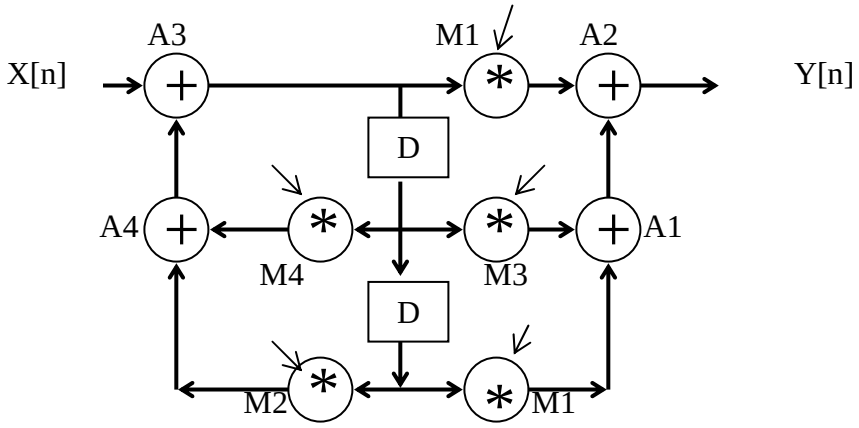
Problem 3 (6 points)

Add these 2 numbers using carry select adders (4-bit)

X=1000 1010
Y=1111 1000
Show the connection between the different 4-bit adders and multiplexters.
Also show the numerical value of every wire assuming the above input

Problem 4 (8 points)

Consider the following circuit. If multiplication takes 2 time units, and addition takes 1 time unit.



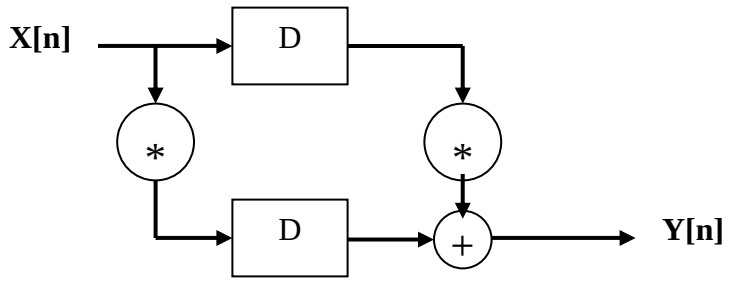
Draw the corresponding SFG (**3 points**)

What is the iteration bound for this circuit (**3 points**)

If that circuit is implemented in hardware, what is the minimum clock cycle? (**2 points**)

Problem 5 (8 points)

Consider the following circuit. Assume that multiplication takes 3 time units, and addition takes 1 time unit.



Write the relation between the input and the output (**3 points**)

Draw the corresponding SFG (**3 points**)

If that circuit will be implemented directly in hardware, what is the minimum clock period? (**2 points**)

Draw a circuit that performs the same function with a smaller clock period (using the same hardware). What is the clock period for your circuit?