York University

Dept. of Computer Science and Engineering

Digital Logic Design

CSE3201

Lab 6

In this lab, you will start designing synchronous sequential circuits.

Problem

1. Implement an S-R Flip Flop using both structural and behavioral model, compare between the propagation delays for both implementation.
2. Implement a D-type Flip Flop with asynchronous reset using both structural and behavioral description.
3. Implement a master/slave JK Flip Flop using both structural and behavioral description.
   For all of the above circuits, demonstrate it using one of the LEDs as an output and the switches as an input.

Preparatory work

Draw the circuit diagrams and write the Verilog code

In the lab

Simulate the circuit, show the simulation result to the TA, and then implement it on the board