York University

Dept. of Computer Science and Engineering

Digital Logic Design CSE3201

Lab 4

The objective of this lab is to get more acquainted with the board, and the Quartus software, You will design, test, and implement a simple circuit.

Problem

Design an 8-bit ripple-carry adder from scratch. Calculate using timing simulation the worst case time to perform an addition.
Then, design a carry lookahead adder, what is the worst case time to add 2 numbers?

Preparatory work

Draw the circuit diagram for both adders, and write the Verilog code for both adders

In the lab

Simulate the circuit, show the simulation result to the TA, then implement it on the board