York University

Dept. of Computer Science and Engineering

CSE3201

Project

Objective:

The objective of this project it to get you some experience with designing moderate digital systems. You are asked to come up with an idea, discuss it with me, design the circuit, implement it and finally test it.

Guidelines

The project is worth 10% of your final mark. The difficulty of the project should also be proportional to that. It must include at least one input/output that is coming/going from/to outside the UP2 board. That could be keyboard, mouse, or any input device. The output should be going to CRT, LCD, LED's or any output device.

Proposal

After checking with me if your idea is worth the 10% dedicated to the project, then write and submit your proposal. The proposal should be 1-2 pages in length. It should describe your idea, and outline what you will do.

Demo

You are asked to demonstrate your project in the last lab session of the year.

Project Report

You are to hand in the project report in the last day of classes. Your report should include the following

1. Description of the project and how to use it
2. Describe your design (components including both software and hardware) and how they are used and connected.
3. Schematics
4. The Verilog code.

The distribution of the marks is as follows 10% for the proposal, 25% for the demo, and 65% for the final report.