

# Digital Logic Design

## Hazards and Glitches

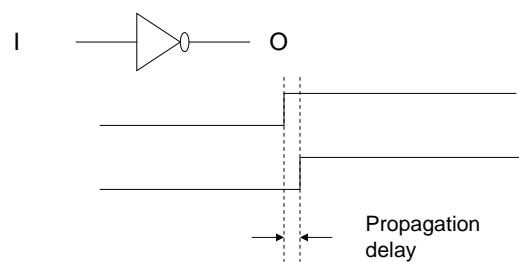
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## Hazards and Glitches

- Gates do not change their outputs instantaneously after changing the input.
- A propagation delay that depends on the gate, Vdd, ...



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# Hazards

$\overline{1} \quad 0 \quad \overline{1} \quad 0$

$0 \quad \overline{1} \quad 0 \quad \overline{1}$

Static 0-Hazard

$0 \quad \overline{1} \quad 0$

$\overline{1} \quad 0 \quad \overline{1}$

Static 1-Hazard

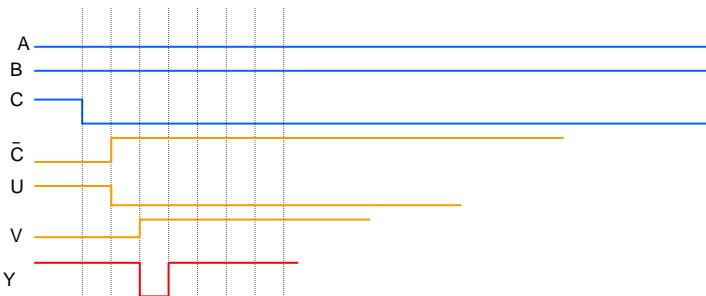
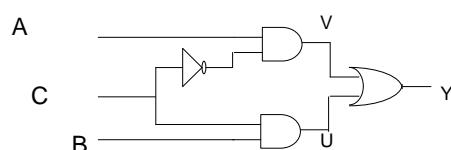
Dynamic Hazards

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## Static Hazards -- Example



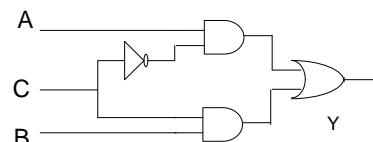
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## Static Hazard -- Example

C \ AB	00	01	11	10
0	0	0	1	1
1	0	1	1	0

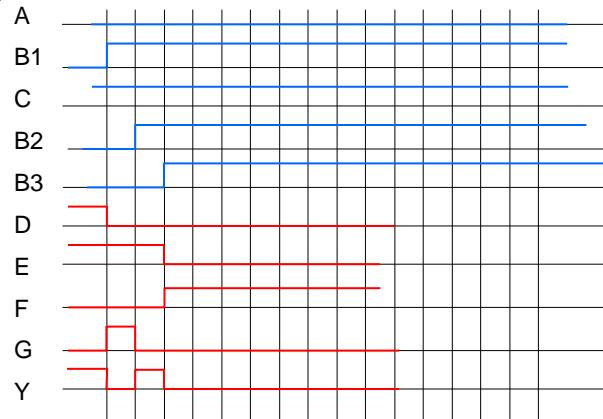
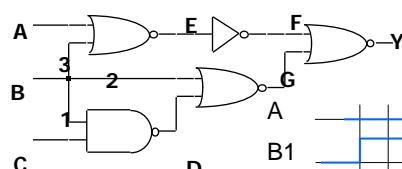


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## Dynamic Hazard



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## Hazards Free Circuits

- For static hazards, we can use K-map and be sure that adjacent 1's are covered by a minterm.
- Not minimum anymore
- No static hazards does not mean no dynamic hazards.
- Best is to design the circuit as a 2-level circuit