Programmable Logic

Programmable logic
• Mask programmable gate arrays and standard cell designs are programmable
  – the user programs the connection patterns
  – High NRE, not reprogrammable, high-volume applications
• Programmable logic usually refers to devices with less NRE and more flexible programming techniques

• Programmable Logic Devices (PLDs)
  – PALs
  – PLAs
• PROM
• Complex Programmable Logic Devices (CPLDs) and Field Programmable Logic Devices (FPGAs)
Simple PLDs

- Devices that can be programmed to implement a wide variety of combinational circuits
- Typically two layers: an ‘AND’ plane and an ‘OR’ plane
  - Can implement sum of products functions
Programmable ROM

- Programmable OR plane selects from all possible minterms
- Decoder maps input pattern to appropriate minterm
- Sum of minterms realisation

PLA Devices

- Programmable logic array device has both a programmable AND plane and a programmable OR plane
- Flexible, efficient implementation of sum of products combinatorial circuits
PAL Devices

- Programmable array logic (PAL) has programmable AND terms and fixed OR plane
- Simpler, better performance than PLA
• PLDs have limited interconnect programmability
• Typically require a special-purpose programmer to program fusible connections
• Field-programmable PLDs incorporate EEPROM style transistors to form/program connections in system
• Limited size and complexity

• Some PAL devices have additional circuitry in addition to or OR gate for each output (a ‘macrocell’)
  – can ‘register’ the outputs
  – feed outputs back as inputs

Functional Logic Diagram ATF22V10C2/CG2
CPLDs

- A large scale device consisting of arrays of simple PLD macrocells.
  - Sum of products
  - Registers to store cell output
  - Clock and control logic
  - Local connections to neighbouring blocks
- Blocks are interconnected through programmable interconnections
• Advantage over PLDs
  – Large number inputs without excessive increase in area (linear versus exponential increase with PLD)
  – Wide ‘fan-in’ on input AND gates
  – 100% connectivity between macro cells allowing complex multilevel circuits
• Electrically reconfigurable (SRAM transmission gates, EEPROM) or OTP

Atmel ATF1500
Max 7000 CPLD

- Altera EEPROM floating gate transistor based CPLD

Main blocks
- Logic Array Blocks (LAB)
  - 36 inputs, 16 output, 16 macrocells with flip-flop and combinational logic
- Programmable Interconnect Array (PIA)
  - Global bus connecting LABs and IOBs
  - Full connectivity with predictable timing
  - Less dense connectivity than FPGA
- I/O blocks
  - Connection/config of pins with PIA and LABs

<table>
<thead>
<tr>
<th>Feature</th>
<th>EPF7Q100</th>
<th>EPF7Q450</th>
<th>EPF7Q150</th>
<th>EPF7Q500</th>
<th>EPF7Q750</th>
<th>EPF7Q1500</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inputs/outputs</td>
<td>32</td>
<td>64</td>
<td>128</td>
<td>192</td>
<td>192</td>
<td>256</td>
</tr>
<tr>
<td>Logic array blocks</td>
<td>2</td>
<td>4</td>
<td>8</td>
<td>16</td>
<td>16</td>
<td>32</td>
</tr>
<tr>
<td>Minimum I/O pins</td>
<td>24</td>
<td>68</td>
<td>100</td>
<td>144</td>
<td>144</td>
<td>192</td>
</tr>
<tr>
<td>Top (I/O)</td>
<td>5</td>
<td>5</td>
<td>6</td>
<td>6</td>
<td>7.5</td>
<td>7.5</td>
</tr>
<tr>
<td>Top (QI)</td>
<td>2.9</td>
<td>2.9</td>
<td>3.4</td>
<td>3.4</td>
<td>4.1</td>
<td>4.1</td>
</tr>
<tr>
<td>Top (QO)</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Max (LQI)</td>
<td>3.2</td>
<td>3.2</td>
<td>4</td>
<td>3.9</td>
<td>4.1</td>
<td>4.1</td>
</tr>
<tr>
<td>Max (LQO)</td>
<td>173.4</td>
<td>173.4</td>
<td>147.3</td>
<td>193.3</td>
<td>193.3</td>
<td>222.2</td>
</tr>
</tbody>
</table>
• LAB consist of macrocells
• Each macrocell
  – Has logic array in form of programmable mini-PAL forming sum-of-products expressions
  – Up to 36 inputs from PIA plus 16 parallel and shared logic expander inputs from neighboring macrocells
  – Flip-flop with programmable input, clocking
Altera 10K Series

- Look up table (LUT) based CPLD devices very similar to FPGAs
- Programmable connection based on SRAM controlled transmission gates
- On chip RAM, higher density, configurability and speed offer more design possibilities than MAX7000

Altera Flex 10K

<table>
<thead>
<tr>
<th>Feature</th>
<th>EPF10K10</th>
<th>EPF10K20</th>
<th>EPF10K30</th>
<th>EPF10K100</th>
<th>EPF10K200</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical gate (logic and I/O)</td>
<td>12,000</td>
<td>20,000</td>
<td>30,000</td>
<td>40,000</td>
<td>50,000</td>
</tr>
<tr>
<td>Memory system gates</td>
<td>35,000</td>
<td>52,000</td>
<td>68,000</td>
<td>33,000</td>
<td>156,000</td>
</tr>
<tr>
<td>Logic elements (LUTs)</td>
<td>674</td>
<td>1,162</td>
<td>1,550</td>
<td>2,048</td>
<td>2,096</td>
</tr>
<tr>
<td>Logic array blocks (LABs)</td>
<td>12</td>
<td>144</td>
<td>216</td>
<td>204</td>
<td>200</td>
</tr>
<tr>
<td>Controlled array blocks (CABs)</td>
<td>5</td>
<td>6</td>
<td>6</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>Total I/O pins</td>
<td>6,144</td>
<td>12,288</td>
<td>13,200</td>
<td>14,304</td>
<td>22,400</td>
</tr>
<tr>
<td>Maximum upper I/O pins</td>
<td>110</td>
<td>150</td>
<td>260</td>
<td>380</td>
<td>910</td>
</tr>
</tbody>
</table>
### Table 2. FLEX 10K Device Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>EPP10K20</th>
<th>EPP10K100B</th>
<th>EPP10K100BA</th>
<th>EPP10K100E</th>
<th>EPP10K100A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical gates (logic and RAM)</td>
<td>70,000</td>
<td>100,000</td>
<td>150,000</td>
<td>200,000</td>
<td>250,000</td>
</tr>
<tr>
<td>Minimum system gates</td>
<td>118,000</td>
<td>158,000</td>
<td>241,000</td>
<td>340,000</td>
<td>540,000</td>
</tr>
<tr>
<td>L2A</td>
<td>5.748</td>
<td>4.105</td>
<td>0.950</td>
<td>10.750</td>
<td>10.750</td>
</tr>
<tr>
<td>L3A</td>
<td>166</td>
<td>264</td>
<td>652</td>
<td>1,630</td>
<td>1,630</td>
</tr>
<tr>
<td>L4A</td>
<td>9</td>
<td>12</td>
<td>18</td>
<td>21</td>
<td>21</td>
</tr>
<tr>
<td>Total RAM bytes</td>
<td>18,142</td>
<td>24,570</td>
<td>52,760</td>
<td>52,760</td>
<td>52,760</td>
</tr>
<tr>
<td>Maximum user I/O pins</td>
<td>168</td>
<td>456</td>
<td>456</td>
<td>456</td>
<td>456</td>
</tr>
</tbody>
</table>

### Figure 1. FLEX 10K Device Block Diagram

![FLEX 10K Device Block Diagram](image)

### Figure 2. EAB Memory Configurations

![EAB Memory Configurations](image)
Field Programmable Gate Arrays (FPGA)

- CPLDs
  - Predictible timing, fewer but large cells
  - Simpler interconnect, place and route easier
- FPGAs
  - More complex, register rich
  - Flexible but complicated interconnections
  - Performance more dependent on routing
FPGAs

- FPGAs are modeled after Mask Programmable Gate Arrays (MPGAs)
- Look-up table based logic elements
- Design to silicon in minutes (or less)
- Dominant technology is SRAM based programming
  - volatile!
  - EEPROM and anti-fuse technologies also exist

Architecture
- Array of programmable logic elements implementing simple sequential and combinational functions
- Fixed but programmable interconnection channels to route signals
- Configurable I/O pin interfaces

Modern devices include
- RAM blocks
- low skew clock distribution and PLLs (critical for high speed clocks)
- flexible I/O standards (for common interfaces)
• RAM based FPGAs programmed by downloading configuration into CMOS RAM
• Downloaded from host or from associated PROM
• Highly reconfigurable but startup time to reconfigure
  – Short programming time facilitates rapid-prototyping

• Bit contents in RAM control state of CMOS transmission gates
  – Program logic elements (functional units)
  – Configure I/O pin function
  – Establish connectivity between logic elements
• Tradeoff between complexity of logic elements and routing resources and wasted cell array/logic elements

FIGURE 8.51 FPGA architecture
FPGA/CPLD resources

- Large designs can be limited by various resources
  - Gates (Marketted as 'equivalent useable gates')
  - Interconnects
  - I/O Pins
  - Memory
- Synchronous designs rely on careful low-skew clock distribution
Design Flow

- Large chips have too many gates for schematic capture
- Hardware description language (HDL) based approaches dominate
- Verilog and VHDL most widely supported and used
- Designs are automatically synthesised from high-level HDL descriptions
IP Cores

- Many vendors provide library and macros or predesigned cores for common operations (multiplexors, ALUs, multipliers …)
- More specialised IP available: network controllers, serial interfaces …
- High end FPGA have significant power and can include capable processors (e.g. NIOS)